AHB Lite SOC Verification

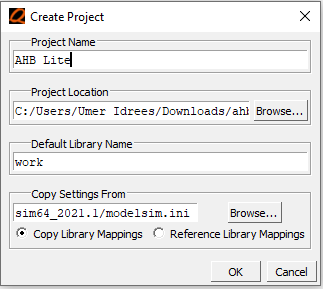
The Verification Plan verify the two design one provided in the class and another from github.

The selection the design is characterized by `define AHB3\_RAM, commenting it out run one design and uncommenting it would run another design. The project files are attached. If not run properly please use the following steps to create a new project.

# Unzip the folder and open Questa Sim and select Create a Project



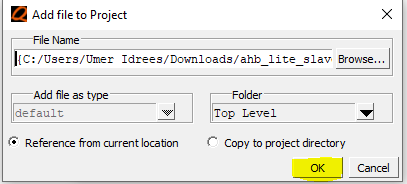
# Create the Project Name as AHB Lite and Default Library Name as Work



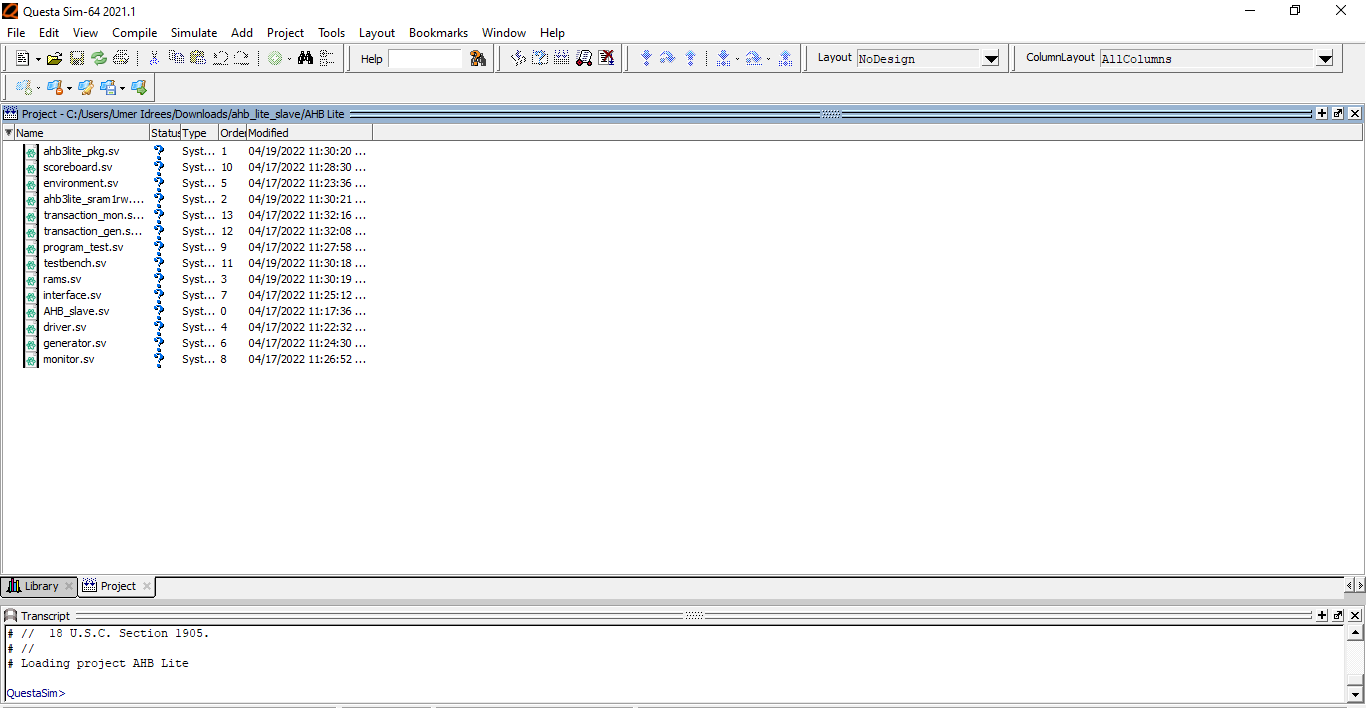
### Click option Add Existing File

# 

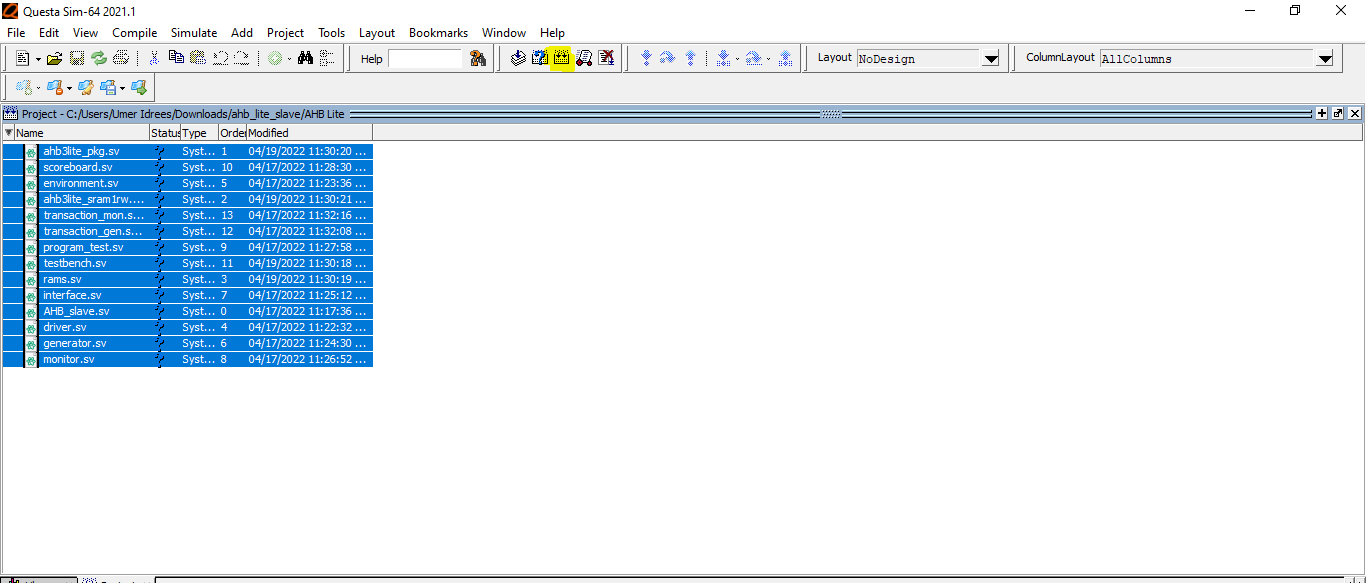
# Add all .SV files from the design and Veri folder



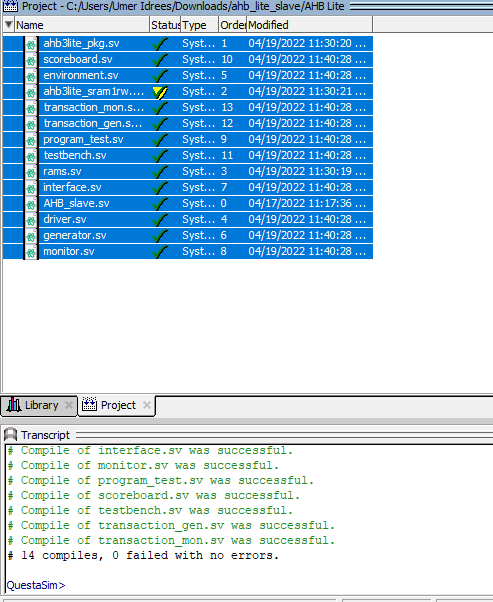
# Verify all the files are open correctly



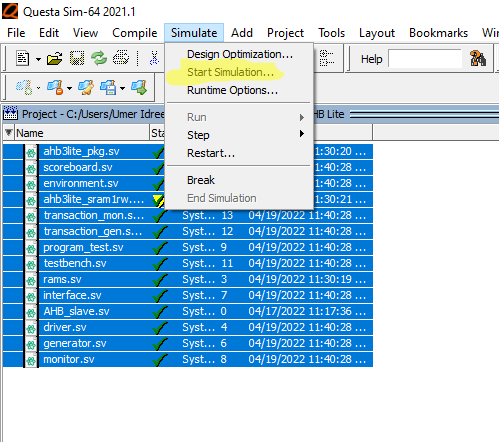
# Select all files and hit compile All button



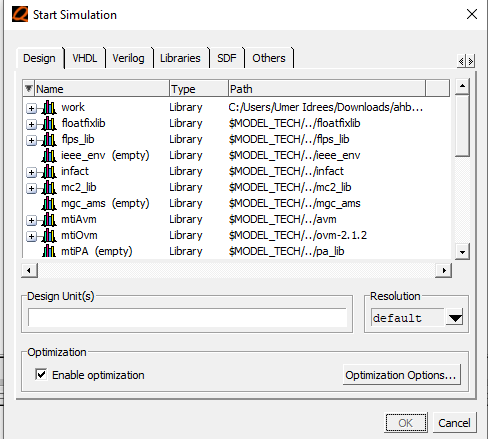
# Verify all the files are compiled without error



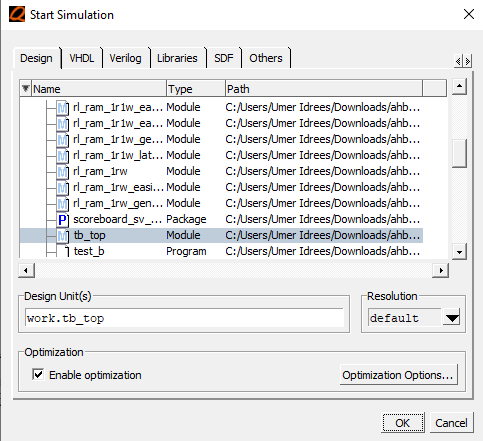
# Go to Simulate and press Start Simulation



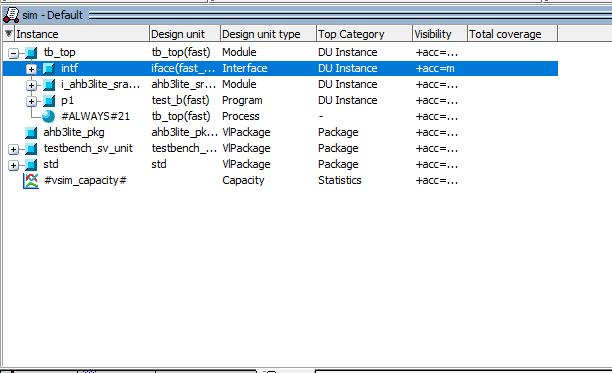
# Verify the following window is open



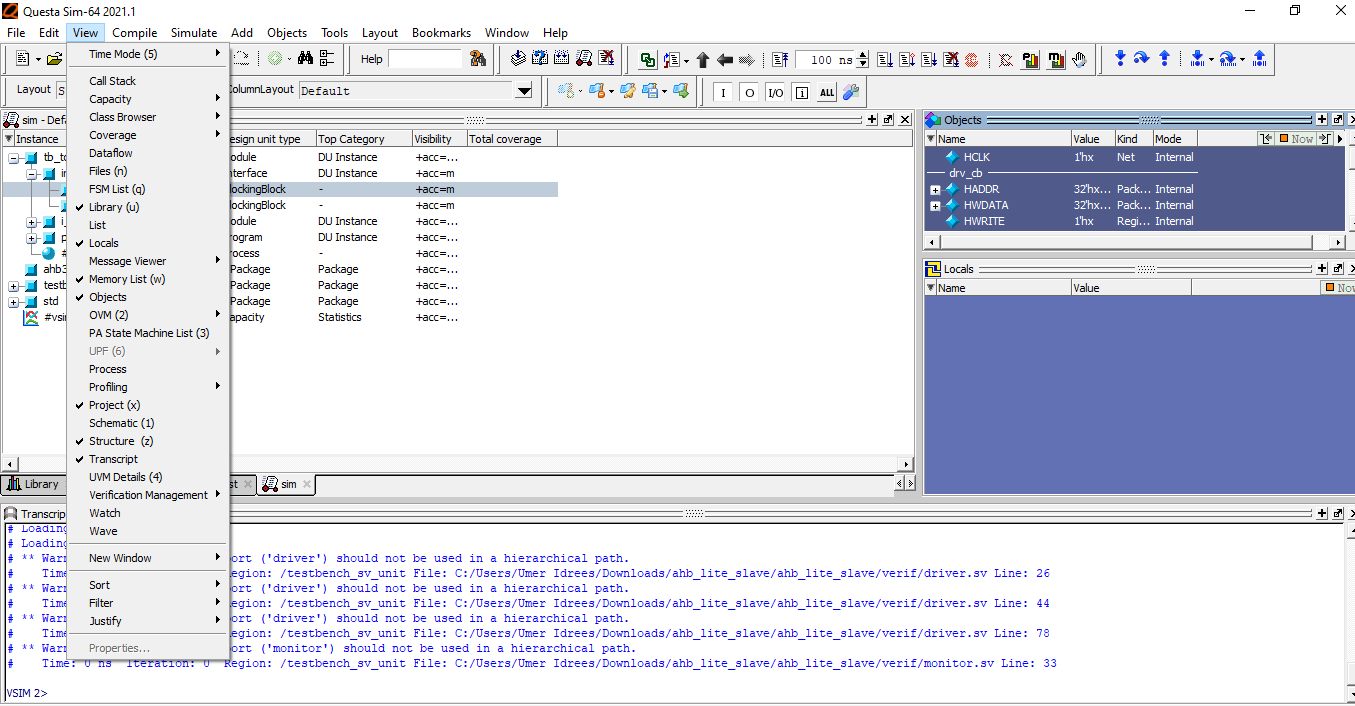
# In the work expand the folder and select the tp\_top Module



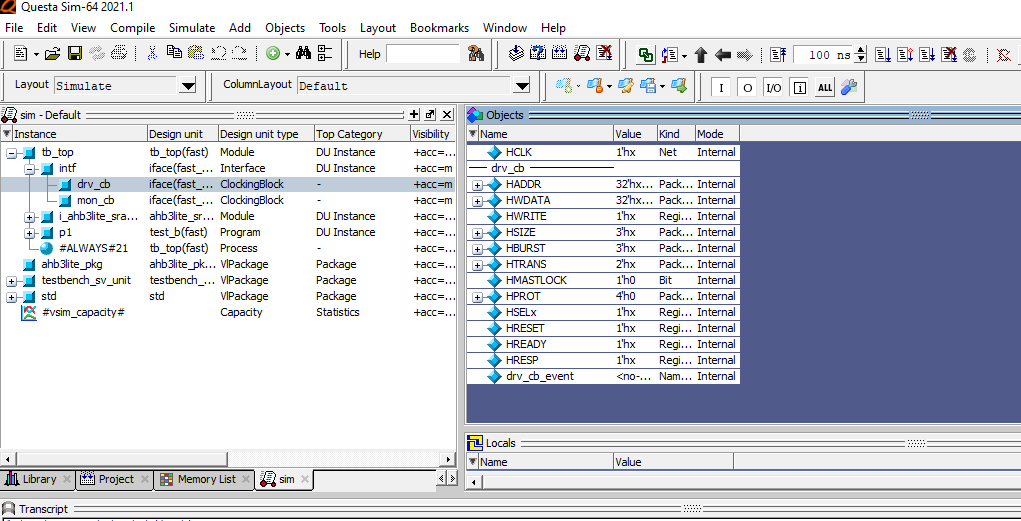
# Verify the Sim log is opened



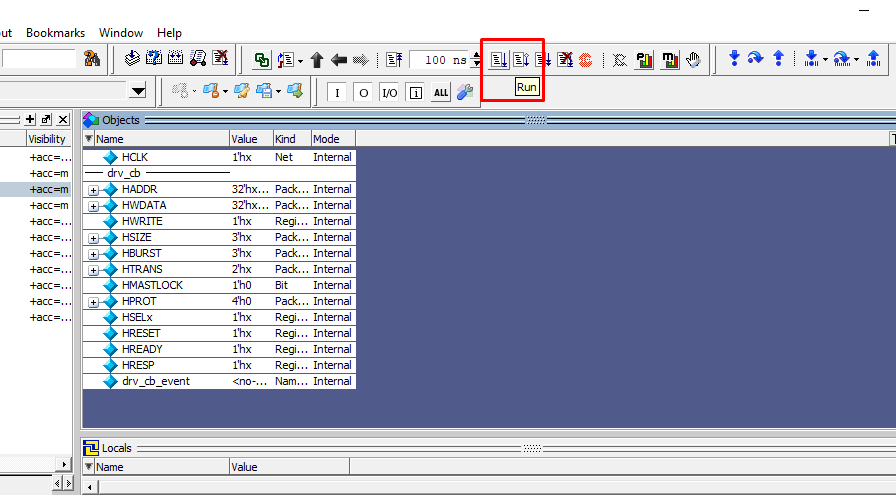
# In the view verify the Local and object are selected.



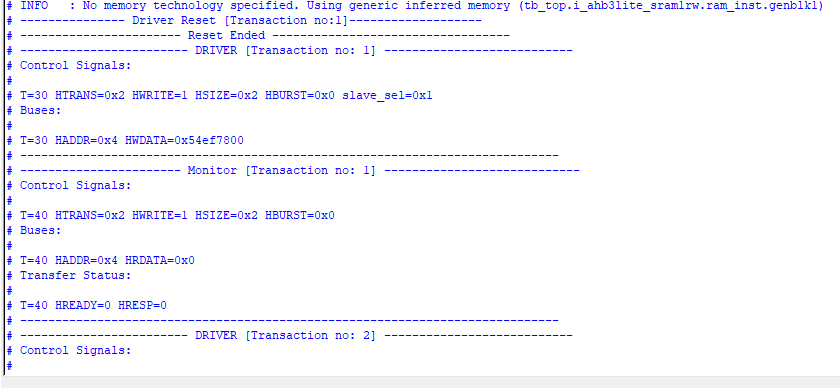
# Select the following in the interface module intf



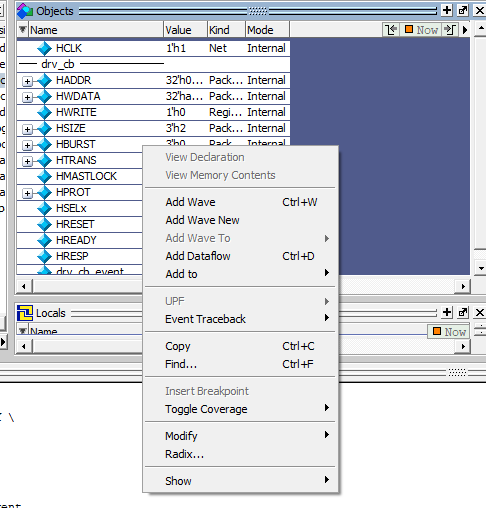
# Select all the signal and hit the run button.



# Verify the transcript block displays all the output

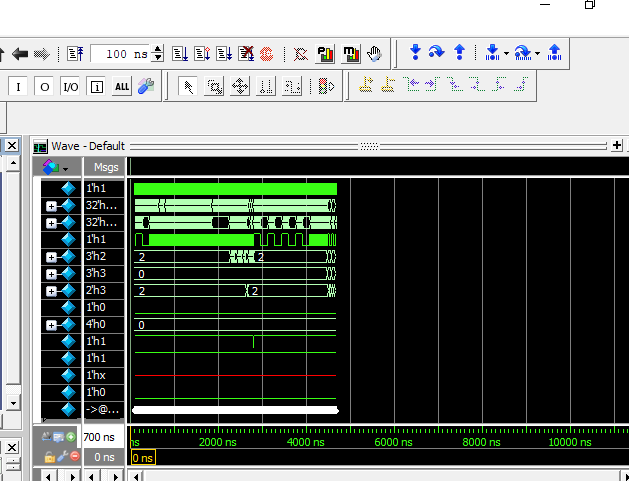


# To observe the Waveform right click and select option Add Wave



# Use the following order changes order Questa Sim sometime throws errors

# Hit the Run button and verify the wave forms are generate for each transcation.



# Use the following order the files changing order Questa Sim sometimes throws exceptions and errors

